Bibliography of BBN documents on parallel processing
(this file was passed to D. Walden by Mike Beeler sometime in 1994 or earlier)

1.0 *MONARCH*

1.1 Monarch External Publications

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1.2 Monarch Internal Publications

"Multiprocessor System Architectures: The Monarch Multiprocessor, vol. 2: Technical Proposal," BBN Labs, November 1984. The only technical description of the Monarch architecture I have been able thus far to locate.

"Dynamic Delay Adjustment: A Technique for High-Speed Asynchronous Communication," BBN Labs, December 1985. Authors: P. Bassett, L. Glasser, R. Rettberg. Presents the circuit-based Dynamic Delay Adjustment (DDA) technique for automatically adjusting signal delays in a MOS system. The technique is characterized by global clock frequency distribution coupled with local, on-chip modems which dynamically adjust the effective delay of data streams between chips. Paper was presented at the Fourth MIT Conference on Advanced Research in VLSI, April 7-9, 1986.

"Shared Memory Parallel Processors: The Butterfly and the Monarch," BBN Labs, April 1986. Author: Randy D. Rettberg. Presented at the Fourth MIT Conference on Advanced Research in VLSI, April 7-9, l986.

2.0 *BUTTERFLY*

2.1 Butterfly External Publications

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"Beyond The Baskett Benchmark," M. Beeler, BBN Author, Computer Architecture News, Association for Computing Machinery, Special Interest Group on Computer Architecture, vol. 12 no. 1, March 1984. Examines criteria for adapting the Baskett benchmark to a multiprocessor and for comparing the results of other benchmarks to the intitial Baskett results on the Butterfly computer.

"A Multiprocessor Implementation of Relaxation-Based Electrical Circuit Simulation," J.T. Deutsch and A. R. Newton, Department of Electrical Engineering and Computer

Sciences, University of California at Berkeley. Published in the 1984 IEEE 21st Design Automation Conference Proceedings.

"Research with the Butterfly Multicomputer," in Computer Science Engineering Research Review, University of Rochester, 1984-85 issue. Authors: C.M. Brown, C.S. Ellis, J.A. Feldman, T.J. LeBlanc, G.L. Peterson -- URI Computer Science Department. See their bibliography.

"Hitchhiker's Guide to the BBN Butterfly," general operating instructions, Thomas J. Olson, University of Rochester, May 1985.

"Getting Started with the BBN Butterfly Multiprocessor," Thomas J. LeBlanc, Computer Science Department, University of Rochester, July 1985.

"Implementation of Finite Element Methods on the Butterfly ™Parallel Processor." BBN Labs, Spring 1985. Authors: H. Allik, W. Crowther, J. Goodhue, S. Moore, R. Thomas. Proceedings of the 1985 ASME International Computers in Engineering Conference, vol. III, American Society of Mechanical Engineers, August 1985. Describes the initial implementation of a set of parallel finite element methods on the Butterfly system and reports almost linear speedup over a range from 1 to 128 processors.

"Performance Measurements on a 128-Node Butterfly™ Parallel Processor," BBN Labs, Spring 1985. Authors: W. Crowther, J. Goodhue, E. Starr, R. Thomas, W. Milliken, T. Blackadar. Proceedings of the 1985 International Conference on Parallel Processing, IEEE Computer Society Press, August 1985. Reports positive results from experiments with two common mathematical algorithms (matrix multiplication, Gaussian elimination solution for simultaneous linear equations) on a 128-node Butterfly machine.

"Getting Started with the BBN Butterfly Multiprocessor," LeBlanc, T.J. and Bukys, L.; University of Rochester, Butterfly Project Report No. 1, Sept. 1985.

"The Butterfly Switch Chip: A User's Perspective on MOSIS," J. Goodhue, P. Bassett, L. Glasser, BBN Labs, 1985. Government Microcircuits Applications Conference Digest of Papers -- First Edition; November 1985. Offers background on the function of the Butterfly Switch Chip and reviews the role of MOSIS as a prototyping shop and supplier of custom-integrated circuits.

Butterfly Project Reports, Computer Science Department, University of Rochester. **(1)** "Getting Started with the BBN Butterfly Multiprocessor," T. LeBlanc, L. Bukys September 1985. **(2)** "A Connectionist Simulator for the BBN Butterfly Multiprocessor," M. Fanty, January 1986. **(3)** "Shared Memory Versus Message=Passing in a Tightly-Coupled Multiprocessor," T. LeBlanc, January 1986. **(4)** "Modula-2 on the BBN Butterfly Parallel Processor," T. Olson, January 1986. **(5)** "NET: A Utility for Building Regular Process Networks on the BBN Butterfly Parallel Processor," E. Hinkelman, February 1986. **(6)** "The Interface Between Distributed Operating System and High-Level Programming Language," M. Scott, March 1986. **(7)** "LYNX Reference Manual," M. Scott, March 1986. **(8)** "SMP: A Message-Based Programming Environment for the BBN Butterfly," T. LeBlanc, N. Gafter, T. Ohkami, July 1986.

"NET: A Utility for Building Regular Process Networks on the BBN Butterfly Parallel Processor," Hinkelman E.; University of Rochester, Butterfly Project Report No. 5, Feb. 1986.

"Finite Element Software on a Multiprocessor," H. Allik and S. Moore, Proceedings of the 9th Conference on Electronic Computation, at U. of Alabama at Birmingham, American Society of Civil Engineers, February 1986. Discusses the continuing implementation and testing of finite element software on the Butterfly Parallel Processor. Describes the organization of the coFEM (concurrent Finite Element Method) program and presents the Uniform System programming methodology.

"LYNX Reference Manual," Scott, M.L.; University of Rochester, Butterfly Project Report No. 7, March 1986.

"The Butterfly™ Lisp System," BBN Labs, May 1986. Authors: S. Steinberg, D. Allen, L. Bagnall, C. Scott. To be presented at the AAAI-86 Conference, Philadelphia, August 1986 and published in the conference proceedings. Describes the Common Lisp system BBN is developing for the Butterfly parallel processor. The system provides a shared heap, parallel garbage collector, and window-based I/O system. The **future** construct is used by the system to specify parallelism.

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"DARPA Parallel Architecture Benchmark Study," Brown, C. et al; University of Rochester, Butterfly Project Report No. 13, Oct. 1986.

"Benchmark Results for Chrysalis Functions," Dibble, P.C.; University of Rochester, Butterfly Project Report No. 18, Dec. 1986.

"Chrysalis++.," Crowl, L.A.; University of Rochester, Butterfly Project Report No. 15, Dec. 1986.

"Experiments with Remote Procedure Call on the Butterfly," Low, J.R.; University of Rochester, Butterfly Project Report No. 16, Dec. 1986.

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"Efficient Implementation of Continuous Speech Recognition on a Large Scale Parallel Processor," Kimball, O., Cosell, L., Schwartz, R., and Krasner, M.; Proceedings of the 1987 International Conference on Acoustics, Speech, and Signal Processing, Dallas, TX, April 1987.

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"Parallel First Fit Memory Allocation," Ellis, C.S., and Olson, T.J.; Proceedings of the 1987 International Conference on Parallel Processing, University Park, PA, August 1987, pp. 502-511.

"Crowd Control: Coordinating Processes in Parallel," LeBlanc, T.J. and Jain, S.; Proceedings of the 1987 International Conference on Parallel Processing, University Park, PA, August 1987, pp. 81-83.

"Recent Developments in Butterfly™ Lisp," Allen, D.C., Steinberg, S.A., and Stabile, L.A.; Proceedings of the 1987 AAAI Conference, Seattle, WA, August 1987; pp. 2-6.

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"Optimization Models for Manufacturing Production Scheduling," Brown, Richard, Shapiro, Jeremy F., and Waterman, Pamela J.; to be published in *Manufacturing Systems*, October 1988.

"Functional Optimization and Pattern Selection in Rayleigh-Benard Convection: An Implementation on the BBN Butterfly™ Parallel Processor," Jeffrey, W., Simon, R., Celmaster, W., Tenenbaum, E., and Rosner, R.; to be published in the Journal of Computational Physics.

"Parallelization of Physical Systems on the BBN Butterfly: Some Examples," Celmaster, W.; to be published in a special issue from the Institute for Mathematics and Its Application, University of Minnesota, Springer-Verlag.

"The BBN Butterfly Used to Simulate a Molecular Liquid," Pawley, G.S., Baillie, C.F., Tenenbaum, E., and Celmaster, W.; to be published Parallel Computing.

"The Uniform System: An approach to runtime support for large scale shared memory parallel processors," Thomas, Robert H. and Crowther, Will; Proceedings of the 1988 International Conference on Parallel Processing, ? , 1988.

2.2 Butterfly Internal Publications

"Computer Architecture Issues for Advanced Memory Technology, BBN Proposal #P75-CSY-49 to ARPA, dated 30 May 1975, proposing a two-man-year general study by the chief architects of the Pluribus system of the ways memories and processors can be configured to gain improved performance through parallelism. Focus of the study to be multi-instruction-stream/multi-data-stream architectures of the next decade. Information contained in this proposal was classified as proprietary at date of issue. Valuable reference document.

"Architecture Study Group Notes" or "ASG Notes, " containing internal memoranda, notes etc. about early design decisions on the Butterfly system. An extra reference set of ASG notes #1-61, covering ASG meeting from January 1, 1976 to December 15, l982, is available thanks to contributors P. Carvey, M. Kraley, W. Milliken, and R. Rettberg.

"A New Multiprocessor Architecture," BBN Report No. #3501, M. Kraley, R. Rettberg, 29 July 1977. An early, if not the earliest external report on the novel Butterfly architecture. "Proprietary" at time of issue. Valuable reference document for history of (or introduction to) BBN's work on multiprocessor design. Contains a literature study and useful early bibliography.

"Development of a Voice Funnel System", BBN Quarterly Technical Reports, vols 1-18 (1978-83) The primary documentation source for Butterfly development. Principal author R.D. Rettberg with M. Hoffman (QTR's 2-5) and J. Goodhue (QTR 16).

"Development of a Voice Funnel System, Design Report," BBN Report #4098, August 1979. This report to DARPA appears not to be a part of the QTR series. Authors are R. Rettberg, C. Wyman, D. Hunt, M. Hoffman, P. Carvey, B. Hyde, W. Clarke, and M. Kraley. Includes chapters on the Voice Funnel Application, the Butterfly Switch, the Processor Node, and System Software. For revisions and changes in details to the Voice Funnel application software presented here, see QTR 14, BBN Report No. 4928, March 1980.

"Butterfly Processor Node I/O Bus Description," BBN Paper, P. Carvey, April 1980.

"Development of A Packet Speech Funnel Multiplexor: A Final Report," May 1982. Author: R. Rettberg. This BBN Report # 4999, covering the period July 1978-July 1981, is part of the Development of a Voice Funnel System QTR series.

"Chrysalis Operating System," BBN Paper, June 1983. Authors: R. Rettberg and R.B. Mann, J. Goodhue, M. Hoffman.

"Development of a Voice Funnel System," BBN Quarterly Technical Reports, vols 1-18 (1978-83) The primary documentation source for Butterfly development. Principal author R.D. Rettberg with M. Hoffman (QTR's 2-5) and J. Goodhue (QTR 16).

"Chrysalis and Processes," on-line discussion and inquiry of the Chrysalis Operating System by Eric Rosen, BBNCC, August 30, l983, with replies by J. Goodhue and B. Mann, September 1983.

"Chrysalis™ Programmer's Manual, Version 2.0," BBN Labs, June 1984. Authors: J. Larus, W. Milliken, J. Goodhue, R. Rettberg, B. Mann, M. Hoffman.

"BUG, The Butterfly User's Guide," BBN Labs, August 1984. Author: Robert J. Walsh. A fairly accelerated short tutorial (3 pgs.) on how to use the Butterfly machine. Use in conjunction with the Chrysalis Programmers Manual (Chrysalis Tools Section).

"Butterfly Development for Strategic Computing." BBN Proposals P84-CSD-027, P84-CSD-027A, and P84-CSD-027B (April, May , and August 1984, respectively). The third proposal appears to update the second, the second the first.

"Chrysalis™ Programmer's Manual, Version 2.1," BBN Labs, November 1984. Authors: J. Larus, W. Milliken, J. Goodhue, R. Rettberg, B. Mann, M. Hoffman.

"Development of a Butterfly Multiprocessor Testbed: Quarterly Technical Report No. 2 (January 16, 1984 - April 15, 1984)." This is BBN Report No. 5873 ; published January 1985. Presents the adaptation of the Baskett Test for use as a benchmark of the Butterfly's performance. Authors are J. Larus and R. Gurwitz.

"The Butterfly High-Speed Gateway: A Draft," BBN Tech Memo CC-0088, W. Mesrobian, BBNCC, January 1985.

"The Design of a Satellite Modem Interface for the Butterfly Satellite IMP," Preliminary Design Report, BBN Labs, January 1985.

"BSAT Design Description," a collection of INFO nodes originally compiled for an internal BSAT design review (February 1985). Compiled, edited, and updated by W. Edmond. A BBN internal document on BBN-VAX.

Butterfly Working Group Notes Series (BWGN), ref. D. Allen, BBN Labs, February 1985. An on-line library exchanging technical information and topics related to the Butterfly Parallel Processor, BBN Labs Inc. The BWGN library resides at a BBN host connected to the DARPA Internet.

"Maintenance and Diagnostics for DARPA Butterfly Multiprocessors: Volume I: Technical Proposal, Volume II: Cost Proposal." (Proposal No. P85-CSD-005). February 1985.

A guide to on-line documentation sources on Butterfly related work compiled by M. Beeler (March 1985). See file "/usr/beeler/doc/sources" for other source file names.

"Butterfly Support for Strategic Computing Applications: Volume I: Technical Proposal, Volume II: Cost Proposal (Proposal No. P85-CSD-041). March 1985.

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"Programming the Butterfly/Multibus Adapter," BBN Labs Manual, March 1985. Author: T. Clarke. Valuable reference document.

"Using the Butterfly To Solve Simultaneous Linear Equations," R. Thomas, BBN author, March 1985. Reports a series of experiments on the Butterfly multiprocessor using the Gaussian Elimination solution method. Part of the project to explore the application of the Butterfly to finite element analysis. See next reference.

"Performance Measurements on a 128-Node Butterfly™ Parallel Processor," Crowther, W., Goodhue, J., Starr, E., Thomas, R., Milliken, W., and Blackadar, T.; IEEE International Conference on Parallel Processing, 1985.

"Butterfly™Parallel Processor Overview," Version 1, BBN Labs, June 1985. Current draft of December 1985.

"Chrysalis™ Programmer's Manual, Version 2.2," June 1985. Authors: W. Milliken, B. Walsh, D. Mankins, R. Tomlinson, M. Beeler and J. Larus, J. Goodhue, R. Rettberg, B. Mann, M. Hoffman.

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"The Uniform System Approach to Programming the Butterfly™ Parallel Processor," Version 1, BBN Labs, October, l985. Current draft of December 1985.

"Behavior of the Butterfly™ Parallel Processor in the Presence of Memory Hot Spots," Robert H. Thomas, BBN Labs, January 1986. The access time for a memory that contains a hot spot is degraded, but the presence of the hot spot has little effect on the performance of programs that avoid the hot memory. Furthermore, tree saturation does not occur in the Butterfly Switch. Paper submitted to the 1986 International Conference on Parallel Processing.

"Butterfly ™Parallel Processor Tutorial for Programming in the C Language," BBN Report No. 6190, March 1986. Author: Michael Beeler. Sections on using and programming the Butterfly computer; appendices in preparation.

"Butterfly™ Parallel Processor Overview," BBN Report No. 6148, March 1986. Authors: R. Thomas, R. Gurwitz, J. Goodhue, D. Allen. Introduction; Architecture; Software Overview; Programming using cooperating sequential processes, the Uniform System, Common Lisp; Other Documentation.

"The Uniform System Approach to Programming the Butterfly™ Parallel Processor," BBN Report No. 6149, March 1986. Version 2; October 10, l986. Authors: R. Thomas, W. Crowther. Introduction; Uniform System Philosophy; Using the Uniform System; Examples; Running and Tuning Uniform System Programs.

"Shared Memory Parallel Processors: The Butterfly and the Monarch," BBN Labs, April 1986. Author: Randy D. Rettberg. Presented at the Fourth MIT Conference on Advanced Research in VLSI, April 7-9, l986.

"APTEC Data Exchange Processor to VME Interface Unit," Technical and Management Proposal, No. P86-CISD-041, BBN Labs to Hughes Aircraft Company, April 1986. Includes a summary of the technical approach to developing the APTEC-VME Interface unit, descriptions of the proposed unit and APTEC microcode, and a discussion of acceptance testing and diagnostic software.

"Butterfly Lisp Reference Manual, April 1986." Edited by C. A. Scott with D. Allen, L. Bagnall, J. Miller, and S. Steinberg. Preliminary release to selected sites to allow early experience coding and debugging parallel algorithms in Lisp and to provide feedback to developers.

Butterfly Workshop Tutorial Package for workshop April 28-May 2, l986. Primarily a compilation of Butterfly slide presentation documents for this workshop only. Includes a workshop schedule of presentations and list of attendees.

"Shared Memory Parallel Processors: The Butterfly and the Monarch," BBN Labs, April 1986. Author: Randy D. Rettberg. Presented at the Fourth MIT Conference on Advanced Research in VLSI, April 7-9, l986.

"Chrysalis™ Programmer's Manual, Version 2.3," May 1986. Authors for this version: M. Beeler, C. Howe, D. Mankins, W. Milliken , R. Schaaf.

"Finite Element Analysis on a Shared-Memory Multiprocessor," H. Allik, S. Moore, E. O'Neil, and E. Tenenbaum, BBN Labs, May 1986. To be presented at the First Annual Congress in Computational Mechanics, University of Texas at Austin, September 1986. To the previously reported results of near linear speedup for matrix multiplication and Gaussian elimination algorithms on a 128-node Butterfly, this paper adds corresponding results for both static and transient Finite Element Method (FEM) calculations using runs of the same implementation (except for actual multiprocessing) on the DEC VAX computer.

"The Butterfly™ Lisp System," BBN Labs, May 1986. Authors: S. Steinberg, D. Allen, L. Bagnall, C. Scott. Presented at the AAAI-86 Conference, Philadelphia, August 1986 and published in the conference proceedings. Describes the Common Lisp system BBN is developing for the Butterfly parallel processor. The system provides a shared heap, parallel garbage collector, and window-based I/O system. The **future** construct is used by the system to specify parallelism.

"The Butterfly Satellite IMP for the Wideband Satellite Network," S. Blumenthal, et al., (Spring 1986). To be presented at the ACM SIGCOMM Conference, Stowe, Vt. Summer 1986.

"The Butterfly™ Satellite IMP for the Wideband Packet Satellite Network," W. Edmond, S. Blumenthal, A. Echenique, S. Storch, T. Calderwood, T. Rees. June 1986. Presented at the ACM SIGCOMM Conference, Stowe, Vt., Summer 1986. Describes the packet switch used in the DARPA Wideband Packet Satellite Network and the Butterfly Multiprocessor on which it is based.

"Use of the Butterfly™ Network Software," BBN Labs, June 1986. Authors: D. Mankins, C. Howe. Introduces design concepts, terminology, and components of the network software with tutorial examples of network routines used in writing programs. Includes concluding section on how to bring up the network software on your machine.

"The Butterfly™ RAMFile System," BBN Report No. 6351, September , l986. Author: Bruce Moxon. Describes a subroutine library that provides application programmers with file-like data access to Butterfly memory. The system uses a set of Unix-like file I/O primitives to support buffered read and write operations at memory access speeds. The RAMFile system also supports parallel read and write operations on this data.

"The Uniform System Approach to Programming the Butterfly™ Parallel Processor," BBN Report No. 6149, October 1986. Authors: R. Thomas, W. Crowther. Introduction; Uniform System Philosophy; Using the Uniform System; Examples; Running and Tuning Uniform System Programs. Includes documentation for Uniform System, Version 2.5, released August 1986.

"Parallelism in the Execution of a Routine Knowledge Rule System on the Butterfly™ Computer," Boulanger, A.; BBN Laboratories Inc., Technical Report No. 6436, December 1986.

"The Butterfly Parallel Processor", BBNACI, January 1987. Compilers: Shawn Spilman and William Downey. This book incorporates all pertinent material from the Voice Funnel Quarterly Technical Reports and other published sources into a detailed technical summary of the Butterfly hardware and software design. The book also provides all the data needed to prepare a site, to bring up a newly installed machine, and to begin using it.

"Application of the Butterfly™ Parallel Processor in Artificial Intelligence," Allen, D.C. and Sridharan, N.S.; Technical Report, BBN Advanced Computers Inc., 1987.

"Parallel Simulation of the Monarch on the Butterfly," Kipnis, S.; Butterfly Users' Meeting, October 1987; BBN Advanced Computers Inc., Cambridge, MA.

"Butterfly MAPLE: A Case Study," Pagan, M. and Geigel T.; Butterfly Users' Group Meeting, October 1987, BBN Advanced Computers, Cambridge, MA.

"An Overview of the Butterfly GP1000: A Large-Scale Parallel UNIX Computer," Howe, Carl D.; International Conference on Supercomputing, Boston, June 1988. (?)

"Porting Molecular Mechanics Software to the Butterfly™ Parallel Computer," Bergsma, John P. and Waterman, Pamela J.; unpublished as of 9/23/1988

"A LISP for the Butterfly ™ Parallel Processor," D. Allen and staff., BBN Labs, (in progress).

"Butterfly Hardware Users Guide" BBN Labs. Authors: T. Blackadar and staff.

3.0 PLURIBUS

3.1 Pluribus External Publications

"The Interface Message Processor for the ARPA Computer Network," F.E. Heart, R.E. Kahn, S.M. Ornstein, W.R. Crowther, and D.C. Walden, first appearance in AFIPS Conference Proceedings, vol. 36, pp. 551-567, June 1970. Also in WW, Chu, Ed, Advances in Computer Communications, Artech House, 1974. Also in P.E. Green & R.W. Lucky, Eds., Computer Communications, IEEE Press, 1975. Also in R.P. Blanc and I.W. Cotton, Eds., Computer Networking, IEEE Press, 1976. Describes the first packet-switch (based on the Honeywell 516) developed by BBN for the ARPA Network. Pre-Pluribus reference document.

"The Terminal IMP for the ARPA Computer Network," S.M. Ornstein, F.E. Heart, W.R. Crowther, S.B. Russell, H.K. Rising, first appearance in AFIPS Conference Proceedings, vol. 40, pp. 243-254, June 1972; also in W.W. Chu Ed., Advances In Computer Communications, Artech House Inc., 1974, pp. 317-328;also in P. Green &

R. Lucky Eds., Computer Communications, IEEE Press, 1975. Pre-Pluribus reference document. Describes the second packet-switch (based on the Honeywell 316, successor to the 516) developed at BBN for ARPA.

"A New Minicomputer/Multiprocessor for the ARPA Network," F.E. Heart, S.M. Ornstein, W.R. Crowther, and W.B. Barker, first appearance in AFIPS Conference Proceedings, vol. 42, June 1973. Also in R.L. Grimsdale & F.F. Kuo, Eds., Selected Papers; International Advanced Study Institute, Computer Communication Networks, University of Sussex, September 1973. Also in W.W. Chu, Ed., Advances in Computer Communications, Artech House, 1974. Called the "initial" Pluribus paper. Presents HSMIMP multiprocessor architecture; choice of processor(SUE), system design (busses etc.), behavior (contention,reliability). Contains early bibliography.

"Reliability Issues in the ARPA Network," W.R. Crowther, J.M. McQuillan, and D.C. Walden; first appears in Proceedings of the ACM/IEEE Third Data Communications Symposium, pp. 159-160, November 1973. Often cited.

"The BBN Multiprocessor," S.M. Ornstein, W.B. Barker, R.D. Bressler, W.R. Crowther, F.E. Heart, M.F. Kraley, A. Michael, and M.J. Thrope; first appears in Proceedings of the Seventh Annual Hawaii International Conference on System Sciences, Computer Nets Supplement, pp. 92-95, January 1974. Pluribus document. Reviews design issues/features of the prototype high-speed IMP as a packet-switching node for the ARPANET (addressing & locking, access enabling, discovery, parity, reloading, mechanical modularity, the test program).

"The Satellite IMP for the ARPA Network," S.C. Butterfield, R.D. Rettberg, and D.C. Walden; first appears in Proceedings of the Seventh Annual Hawaii International Conference on System Sciences, Computer Nets Supplement, pp. 70-73, January 1974. "No real relevance to Pluribus," I am told. Describes an implementation of the first satellite IMP built on 316 hardware. Paper often cited in later PSAT papers.

"Pluribus -- A Reliable Multiprocessor," S.M. Ornstein, W.R. Crowther, M.F. Kraley, R.D. Bressler, A. Michael, and F.E. Heart; first appears in AFIPS Conference Proceedings, vol. 44, pp. 551-559, May 1975. Key Pluribus document. First discusses multiprocessor architecture; then reliability goals and strategies, including multiple copying of algorithm resources, simplicity, dealing with redundancy, and use of watchdog timers; and, finally, system relability mechanisms as applied to example system failures.

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"Pluribus: A Multiprocessor for Communications Networks," R.D. Bressler, M.F. Kraley, and A. Michel; first appears in 14th Annual ACM /NBS Technical Symposium --

"Computing in the Mid-70's: An Assessment," pp 13-19, June 1975. Describes Pluribus hardware and software design philosophy, discusses reliability strategies, and presents actual and potential applications of the Pluribus line. These applications include Pluribus IMPs, Satellite IMPs, a Communications and Control Processor (CCP), Private Line Interfaces (PLIs), Front-End Processing, and a Pluribus Terminal IMP (TIP).

"The Evolution of a High Performance Modular Packet-Switch," S.M. Ornstein and D.C. Walden; first appearance in Conference 1975 International Conference Communications, vol. 1, pp. 6-17 to 6-21, June 1975. Profiles BBN's several-year effort (1968-74) to build packet-switches. Describes the original pair of switches based on the Honeywell 516; the later, less expensive 316 version; and the new Pluribus. Reference document to the period.

"A Network-Oriented Multiprocessor Front-End Handling Many Hosts and Hundreds of Terminals," W.F. Mann, S.M. Ornstein, and M.F. Kraley. First appears in AFIPS Conference Proceedings, vol. 45, pp. 533-540, June 1976. Key multiprocessor document. The design and system requirements of a large-scale front-end computer, based on the design of the Pluribus, is contrasted with the design of the ARPANET TIP.

"The Pluribus Multiprocessor System," F.E. Heart, S.M. Ornstein, W.R. Crowther, W.B. Barker, M.F. Kraley, R.D. Bressler, and A. Michael; first appears in Multiprocessor Systems: Infotech State of the Art Report, Infotech International. Ltd., pp. 307-330, 1976. This paper was compiled, with some amendments, from copyright material contained in "A New Minicomputer/Multiprocessor for the ARPA Network," F.E. Heart et al (1973) and "Pluribus -- A Reliable Multiprocessor," S.M. Ornstein et al (1975). I have on loan a copy of the entire Infotech report.

"Communications Applications of the Pluribus Computer," F.E. Heart and D.C. Walden; appears in the Conference Record of the 1976 IEEE National Telecommunications Conference, Dallas, Tx. Nov. 29 - Dec 1, l976, pp. 7.1-1 to 7.1-5. Introduces the Pluribus, discusses its suitability for communications applications, presents seven applications where a Pluribus system has been or will be used, and notes the current operational status of Pluribus systems (5 in field operation; 5 constructed and awaiting delivery; several more used for software and hardware development and system fabrication and testing).

"Software Fault-Tolerance in the Pluribus," J. Robinson, and E. Roberts, appears in AFIPS Conference Proceedings, vol. 47, June 1978, pp. 563-569. Contrasts new "relaxed reliability" application techniques in the Pluribus operating system with classical approaches to fault-free reliability. Presents the "stage" operating system in the Pluribus.

"Pluribus -- An Operational Fault-Tolerant Multiprocessor," D. Katsuki, E. Elsam, W. Mann, E. Roberts, J. Robinson, F. Skowronski, and E. Wolf; first published in IEEE Proceedings, pp. 1146-1159, October 1978. Key paperdescribing several techniques used to achieve fault-tolerance in the Pluribus multiprocessor system. Includes history and review of 8 Pluribus IMP field systems.

"The Pluribus Fault-Tolerant Multiprocessor," J. Robinson, in Proceedings of COMPCON 79 Spring Proceedings (Spring 1979), pp. 45-48.

"Software Techniques for Practical Multiprocessors," E. Roberts, Ph.D. Thesis in Applied Mathematics, Harvard University, May 1980. Explores problems of parallel control facilities for multiprocessor systems and presents techniques to simplify development of efficient software in a multiprocessor environment. Includes a survey of the Pluribus, a critique of the rendezvous mechanism in ADA, and presents a process/event model for a high level language and/or ADA.

"A Multiprocessor Channel Scheduler for the Wideband Packet Satellite Network," G. Falk, S. Groff, W. Milliken, M. Nodine, S. Blumenthal, and W. Edmond. First presented at IEEE International Conference on Communications, Boston, June 19, 1983. Describes Wideband Network services supported by the PSAT, and presents an overview of PSAT algorithms, hardware, and software.

"Integration of Voice and Data in the Wideband Packet Satellite Network," same authors. Appears first in IEEE Transactions on Communications, 1983, and also in IEEE Journal on Selected Areas in Communications, December 1983. The Wideband (packet satellite) network is being used to evaluate the use of packet transmission for efficient voice communication, voice conferencing, and integration of voice and data over a satellite channel. This paper, which revises "A Multiprocessor Channel Scheduler for the Wideband Packet Satellite Network" (June 1983), describes the protocols and mechanisms upon which the Wideband packet satellite network is based.

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Network" (June 1983), describes the protocols and mechanisms upon which the Wideband packet satellite network is based.

Note: Related key documents. D. Katsuki et al., "Pluribus -- An Operational Fault-Tolerant Multiprocessor," October 1978. Discusses the implementation of the PSAT application on the Pluribus. See above, page 3. Also R.D. Rettberg et al., "Development of a Voice Funnel System: Design Report," BBN Report No. 4098, August 1979, below in the Butterfly period section of this bibliography. Presents the adaptation of the PSAT application to the Butterfly multiprocessor.

"Experiences in Building a Wideband Packet Satellite Network," BBN author S. Blumenthal, paper presented at NETWORKS 85' London and reproduced by Online Publications, Pinner, UK, 1985. Includes an "overview" and "current status" sections, along with a discussion of systems design and integration issues that have arisen during the development of the Wideband Network and, finally, a section on "network management tools." A version of this paper, entitled "Arpanet Hitches a Satellite Ride," was published in Communications Systems Worldwide, September 1985.

"A Network-Oriented Multiprocessor Front-End Handling Many Hosts and Hundreds of Terminals," W.F. Mann, S.M. Ornstein, and M.F. Kraley. First appears in AFIPS Conference Proceedings, vol. 45, pp.533-540, June 1976. Key multiprocessor document. The design and system requirements of a large-scale front-end computer, based on the design of the Pluribus, is contrasted with the design of the ARPANET TIP.

3.2 Pluribus Internal Publications

Combined Quarterly Technical Reports 7-37, including the "Pluribus Satellite IMP Development," reports, covering the period 1972-1985. The relevant CQTR's are listed here chronologically by name of principal BBN author. **R. Bressler** CQTR's #7 -23: See #7 BBN Report No. 3722 (Nov 1977); #8, No. 3767 (Feb 1978); #9, No. 3824 (May 1978); #10, No. 3911 (Aug 1978); #11, No. 3984 (Nov 1978); #12, No. 4068 (Feb 1979); #13, No. 4133 (May 1979); #14 , No. 4184 (Aug 1979); #15, No. 4279 (Nov 1979); #16, No. 4342 (Feb 1980); #17, No 4399 (May 1980); #18, No. 4474 (Aug 1980); #19, No. 4526 (Nov 1980); #20, No. 4609 (Feb 1981) missing; #21, No. 4679 (May 1981); #22, No. 4761 (Aug 1981); #23, No. 4825 (Nov 1981). **J.F. Haverty** CQTR's #24-29: See #24, No. 4868 (Feb 1982); #25, No. 5003 (May 1982); #26, No. 5129 (Aug 1982); #27, No. 5215 (Nov 1982); #28, No. 5286 (Feb 1983); #29, No. 5345 (May 1983). **S. Blumenthal** CQTR's #30-37: See #30, No. 5408 (Sept 1983); # 31, No. 5492 (Nov 1983); #32 , No. 5580 (Feb 84); 33, No. 5774 (May 1984); #34, No. 5797 (Aug 1984);#35, No. 5883 (Nov 1984); #36, No. 5977 (Feb 1985); #37, No. 3992 (May 1985).

HSMIMP Notes. Index and permuted Index for Notes 1-328. HSMIMP Notes 1-425 were created. The memos span the period 20 June 1972 to 19 January 1981. The latest notes include discussion of shortcomings from the programmer's point of view. Some of the ideas went into the Butterfly -- John Robinson. Reference: the notes cannot be found in the BBN Libraries. John Robinson's collection of HSMIMP notes lacks only numbers 258, 271, 348, 379, 396, 414, 416, 419, 423.

Photographs of Pluribus (and PTIP and HSMIMP) have been archived by Bob Brooks (x3453). These photos include technical and more informal shots.

"Proposal for Development, Implementation, and Installation of the Communication and Control Processor for a Seismic Network," BBN Proposal No. P74-CSY-26, 22 May 1974. Based on the new Pluribus multiprocessor architecture, the CCP is proposed as the data collection and routing center for on-line seismic data collection as well as the network control center for the seismic network (VELA).

"Use of the ARPA Network by the Seismic Data Collection Network," BBN Report 2995, H. Briscoe Principal Investigator, 30 January 1975. The report that first recommended adding Pluribus IMPS to the Arpanet to solve certain performance problems that would occur if the seismic data network used the Arpanet. A detailed analysis of the data flow paths in the Arpanet indicated several areas where the network would have to be expanded to accommodate the large amount of anticipated seismic data. Reference note: BBN Report 2995 was incorporated into BBN Report 3109, "Final Report: A Study of Communications for the Seismic Data Collection Network," H. Briscoe, Principal Investigator, 30 June 1975.

"Final Report: A Study of Communications for the Seismic Data Collection Network," BBN Report No. 3109, H. Briscoe, Principal Investigator, 30 June 1975. Reports the results of four engineering "tasks" or studies intended to verify the design and support the implementation of the seismic data collection network, concentrating in particular on the communication subsystem and especially on the ARPA network paths.

"Issues in Packet Switching Network Design," W. Crowther, F. Heart, A. McKenzie, J. McQuillan, and D. Walden, presented at the National Computer Conference, 1975. Covers in detail the three major areas where key choices must be made in designing a packet-switching network: network hardware design, store-and-forward subnetwork software design, and source-to-destination software design. Valuable reference document.

"Programmable Reliability in a Multiprocessor," S.M. Ornstein, W.R. Crowther, and M.F. Kraley. Unsure as to first appearance or date of publication, if published or presented. Postdates previous Pluribus paper, probably circa 1975. Discusses a "highly adaptive" software approach to fault detection in a shifting hardware environment. I have one hard copy.

"A Multiprocessor Design," W.B. Barker, October 1975 . This manuscript, BBN Report #3126, was submitted by the author as his doctoral thesis at Harvard University. Ben Barker is also supplying us with some introductory material to the thesis that did not appear in the BBN report.

"Acceptance Test Procedures for the Communications and Control Processor," BBN Report 3185, H. Briscoe, Principal Investigator, 9 April 1976. Document defines tests that demonstrate the useable features of the 4-processor CCP, installed at the Seismic Data Analysis Center in July 1975. Acceptance tests were begun in November 1975 and completed in February 1976. Five phases of testing are described, including the HIT

hardware test program (a general Pluribus system test configuration program), the operational program, reliability, system operation, and demonstrate editor and assembler.

"Pluribus IMP Test and Evaluation Plan," BBN Report No. 3336, R. Gudz and H. Rising, July, l976.

"Implementation and Acceptance Testing of the Seismic Communication and Control Processor," BBN Report No. 3349, H. Briscoe, Principal Investigator, 9 August 1976. An interim report prepared for the VELA Seismological Center.

"Interim Report on Refinements and Operator Training for the Seismic Communication and Control Processor System (CCP)," BBN Report No. 3444, H. Briscoe, Principal Investigator, 18 November 1976. Also prepared for the VELA Seismological Center. Reviews three training courses, maintenance assistance, and software refinements to the operating system.

"Application of the Pluribus Multiprocessor in a Distributed Data Collection and Processing Network," R. Gudz, January 10, l977. Searching for this report.

"Final Report: Pluribus IMP Test and Evaluation Project," BBN Report # 3523 to NSA; 31 March 1977, no authorship cited. Report does not appear in 1982 bibliography of Technical Reports on the ARPANET Project (BBNCSD). I have one hard copy on loan and am making additional copies.

"Platform Satellite Extension," BBN Technical Proposal P77-CSV-20C, March 1977. Proposes to add three Pluribus IMPs to the NSA Platform Network, which now (1986) has the largest concentration of Pluribus hardware in existence. The Platform Network became all-Pluribus around 1979 or 1980. Updates proposal P77-CSY-20 of October 1976.

"VELANET Communications Control Processor Computer Product Specification Final Software Documentation, BBN Report No. 3329, March 15, l977.

"Interim Report on Phase I Expansion of the Seismic Communication and Control Processor System (CCP)," BBN Report No. 3531, H. Briscoe, Principal Investigator, April 1977 Reviews implementation and acceptance testing of Phase I hardware and software expansion of the CCP in December 1976 and January 1977. This first phase of upgrading of the CCP included increasing private and shared memory in the CCP, designing and coding input software for leased line North American Network stations, and a design study for buffered interface hardware for leased line data.

PLUDOC 1: "Overview," BBN Report No. 2999, May 1975, is useful. Also PLUDOC 2: "System Handbook," BBN Report No. 2930, update edition of April 1977, authors C.R. Morgan, M.F. Kraley. An attached "Introduction to Pluribus Documentation" by R.A. Tilden (March 1979) describes the seven -volume Pluribus Document Series and the two-volume ARPANET Pluribis IMP Program Report (TIR 97,99, May 1978), defining the STAGE system implemented in current Pluribus applications. Tilden also mentions a series of earlier working papers known as "HSIMP Notes," profiling the motivation

behind early multiprocessor development. Tilden's notes include a guide to PLURIBUS on-line documentation as of 1978.

"VELANET Communication Protocols between the CCP and SIP and between the CCP and DP," BBN Report No. 3460, H. Briscoe, Principal Investigator, 5 April 1977. Describes revised protocols and formats for communication over the ARPANET between the CCP, acting as the central node in the VELANET, and the Seismic Input Processor at CCA and between the CCP and the Detection Processor.

"Final Report on Phase II Expansion of the Seismic Communication and Control Processor System (CCPP)," BBN Report No. 3686, H. Briscoe, Principal Investigator, November 1977. Reviews the second phase of upgrading to include an increase in the number of processors in the CCP, replacing the 6 SLI boards with 6 buffered SLI boards, making appropriate changes to operational and test software, and modifying the communication protocol software to accommodate a new NORSAR format and improved ARPANET interaction.

"ARPANET Completion Report," an ARPA report prepared at BBN by D. Walden , A. MacKenzie and staff, January 3, l978. Contains an executive summary, formal completion report, history and review of the ARPANET project, and a BBN ARPANET bibliography. The September, l977 draft of this report has additional sections on the ARPANET design and implementation, experience in use and operations, and observations.

"The ARPANET Pluribus IMP Program," BBN Technical Information Report 97 (also 99) Vol I: Introduction. The IMP Algorithm, the STAGE System. Vol 2: DDT, Program Descriptions, Data Formats. May 1978. Possibly revised since.

PLUDOC 3: "Configurator," (not listed in TRAP bibliography). PLUDOC 4: "Basic Software," BBN Report No. 3001, a revision dated September 1978, including SUE instruction set; assembler introduction; DDT. PLUDOC 5: "Advanced Software," BBN Report No. 2931, a revision dated September 1977, including Lockheed software; assember manual. PLUDOC 6: "Functional Specifications," BBN Report No. 3002, a revision dated September 1977. PLUDOC 7: "Maintenance," BBN Report No. 3004, a revision dated September 1977.

TIPMEM Series. Numbered 1-20 and dated 26 October 1978 to 17 April 1980. These notes describe some aspects of the PluribusTIP/PTIP (and Honeywell TIP) software structure. John Robinson's set is incomplete. Not in library.

"Final Report: The Impact of Multiprocessor Technology on High-Level Language Design," BBN Report No. 4188, BBN authors A. Evans Jr., C. Morgan, E. Roberts, with E. Clarke (Harvard), January 9, l979.

"Pluribus TIP Users' Guide," BBN Report No. 4135, N. Mimno, June 1979.

"Analysis of System Considerations for the Wideband Packet Satellite Network Channel," BBN Report No. 4179, J. Mayersohn, I. Richer, and E. C. Rosen, August 1979. Discusses some possible performance problems in the Wideband Network

protocols and algorithms, and in the Pluribus architecture itself running the Wideband Network application (PSAT). Topics: Congestion Control, Priority and Delay Class, End-to-End Flow Control, Pluribus Throughput.

"The Pluribus Multiprocessor," A. Michel, J. Cherniack, and P. Ressler, in or at the National Electronic Conference, Chicago, IL., October 1979. Four-page introduction to the Pluribus system based on its 5 year field record as an IMP in the Arpanet.

The following five items are best seen as a series -- a three report study of the Pluribus's performance limits and means to improvements, followed by two proposals to fund and do some of the improvements. No funding yet. In some places we borrowed ideas from the Butterfly design in the proposed improvements -- John Robinson. **(1)** "Pluribus Study Progress Report," BBN Report No. 4447, R. Nelson, J. Robinson, S. Skowronski, G. Williams, D. Katsuki, June 1980. **(2)** "Pluribus Study Draft Final Report," BBN Report No. 4324, same BBN authors plus P. Sevcik, October 1980. **(3)** "Pluribus Study Final Report," BBN Report No. 4585, same BBN authors plus R. Alter, J. Goodridge, and P. Sevcik, January 1981. **(4)** "Pluribus and NOC Improvements," BBN Proposal P82-CCO-009, October 1981. **(5)** "Pluribus IMP Hardware and Software Enhancements," BBN Proposal P83-COM-26, October 1982.

"History of the ARPANET: The First Decade," BBN Report 4799, R. Bressler, April 1981.

"PSAT Technical Report", BBN Report No. 4469, G. Falk, S. Groff, R. Koolish, W. Milliken, May 1981. Reference document. Note: the Host Access Protocol (HAP) specification presented in Chapter 4, has been superceded by RFC 907, "Host Access Protocol Specification," July 1984. The revisions to the original specification are described as "minor" and include the definition of three new control message types (Loopback Request, Link Going Down, NOP), a "Reason" field in Restart Request control messages, new Unnumbered response codes, and new values for the setup codes used to manage streams and groups. HAP is described as an experimental protocol which will undergo further revision as new capabilities are added and/or different satellite networks are supported.

"PSAT Software Report," BBN Report No. 4622, G. Falk, S. Groff, R. Koolish, W. Milliken, July 1981. Reference document.

"OPSN Design Study -- Final Report," BBN Report No. 4772, G. Williams, P. Sevcik, A. Huang, September 1981. OPSN was the second all-Pluribus network installed at NSA.

"Technical Reports on the ARPANET Project." A bibliography of public documents produced by BBN about Pluribus-like machines and others as of January 1982. Issued by BBN Computer Systems Division. Does not include listings of internal documents, such as HSIMP notes or QTR's published after ARPA left the project. Most, but not all, of the documents selected for this multiprocessor bibliography are also listed with many others in the TRAP bibliography. The abstracts of the QTR's listed from 1969 to 1976 give a chronology of the IMP, TIP, Satellite IMP, HSIMP, and Pluribus IMP programs. Pluribus-related reports from BBN are also included in the "Other Reports" section of

the TRAP bibliography. Thanks go to M. Bremer and B. Brooks for forwarding copies of it.

"Pluribus Satellite Interface Message Processor (PSAT) Site Planning and Installation Guide," BBN Report No. 5186, S. Blumenthal, G. Falk, October 1982. Reference document.

"Development of Packet Satellite Networking Technology: A Final Report for Contract No. MDA903-76-C-0252," BBN Report, No. 5266, first author G. Falk, January 1, l983. Searching.

PSAT Notes. Numbered 1-43 and dated 28 October 1977 to 10 December 1984. The notes describe the Pluribus Satellite IMP (PSAT) program for the Wideband Network. John Robinson has an incomplete set. Walter Milliken has donated his set to us comprising notes 5-43. Not in library.