United States Patent [19]

Rettberg et al.

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[54] **DIGITAL PHASE ADJUSTMENT**

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[51] **Int. Cl.**[4] **G06F 11/00**

[52] **U.S. Cl.** **371/1;** 328/55

[58] **Field of Search** ..... 371/1, 25; 328/55, 56; 364/200, 900; 324/73 R

[56] **References Cited**

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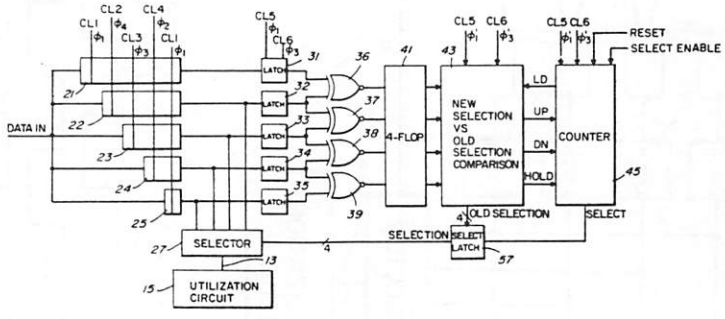
[57] **ABSTRACT**

In the apparatus disclosed herein, a data signal to be phase adjusted is applied to a plurality of delay lines providing progressively greater delays. The outputs of the several delay lines are compared over a period of time and a selection of one of the output signals for utilization is made based on choosing that delay line output which is in opposition to that pair of outputs which straddles or encompasses the most transitions.

7 Claims, 9 Drawing Figures



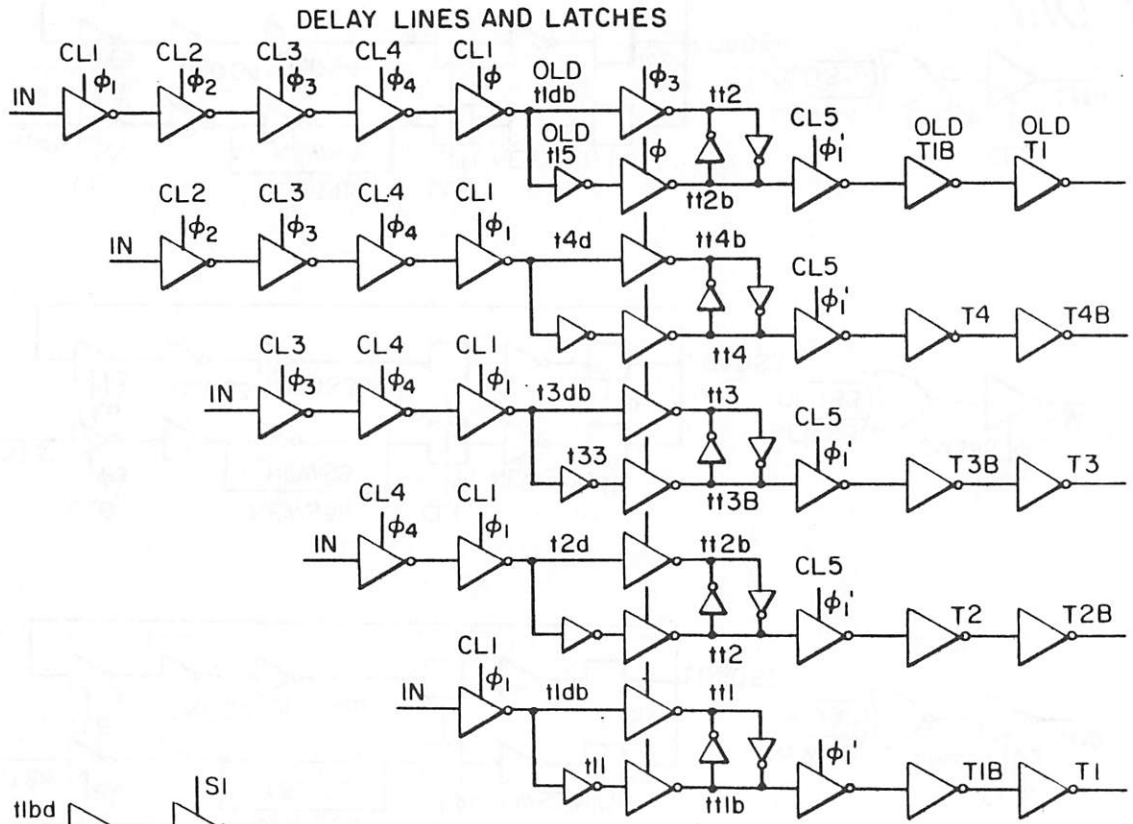


FIG. 3

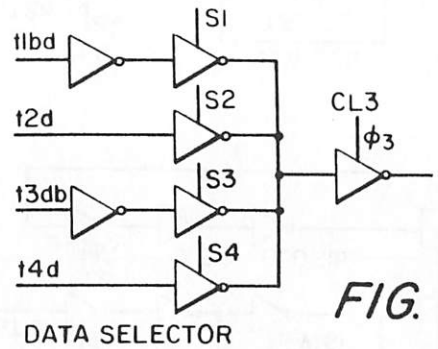


FIG. 2

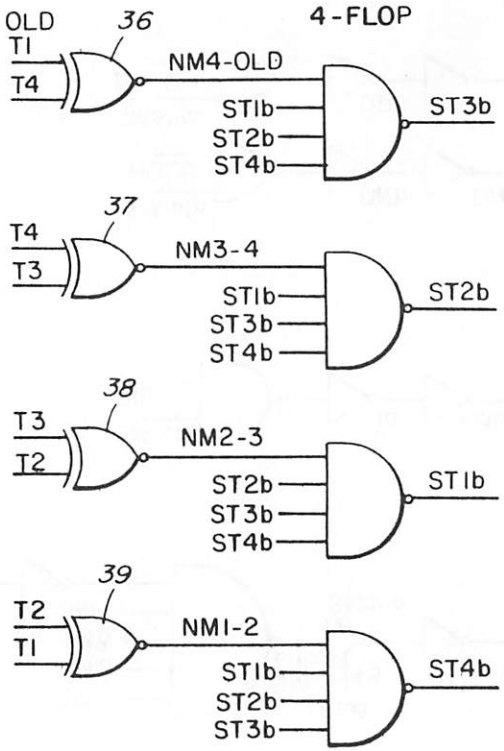


FIG. 4

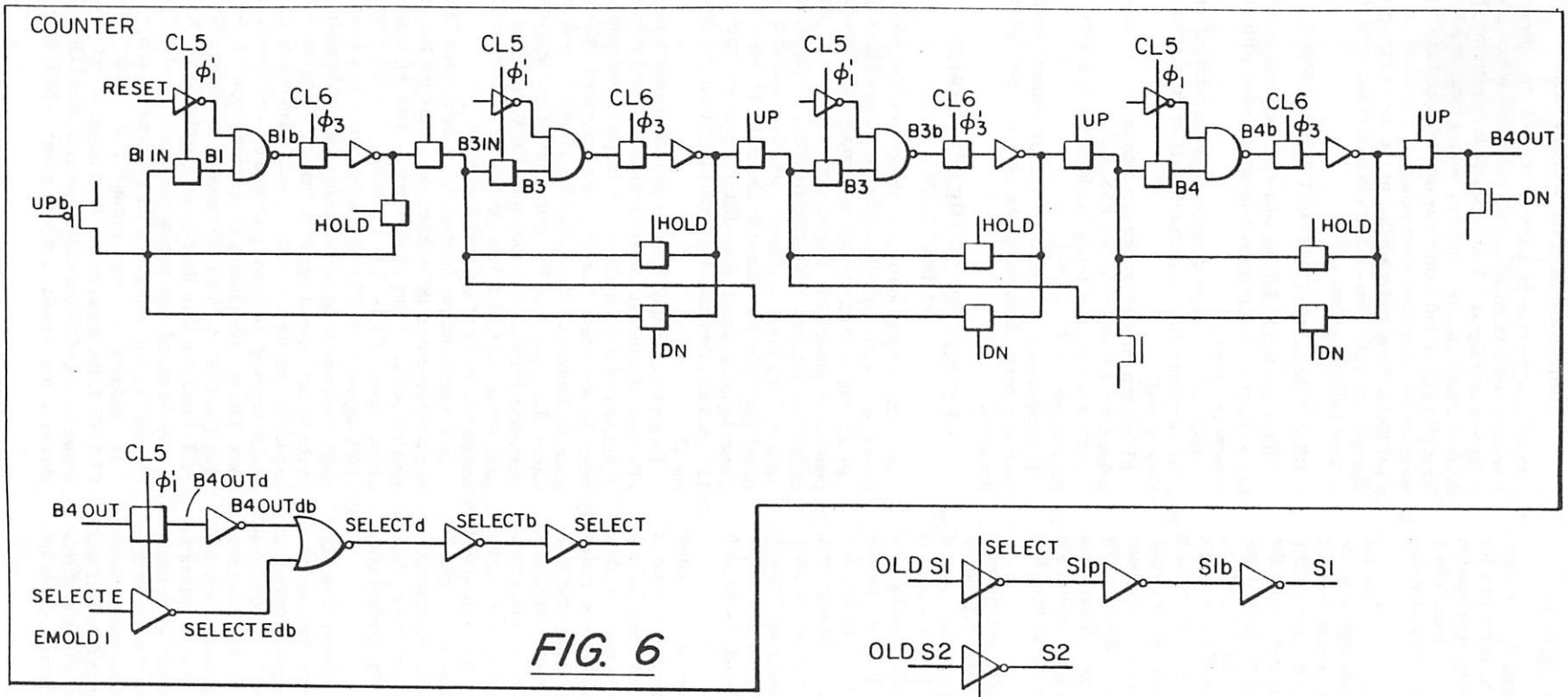

COUNTER
CL5
ϕ_1'
RESET
CL6
ϕ_3
B1 IN
B1
B1b
HOLD
UPb
B3IN
B3
B3b
UP
DN
B4
B4b
B4OUT
CL5
ϕ_1
B4 OUT
B4OUTd
B4OUTdb
SELECTd
SELECTb
SELECT
SELECTE
EMOLD I
SELECTEdb

FIG. 6

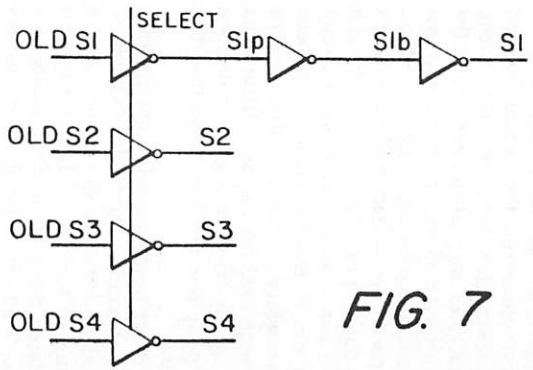

SELECT
OLD SI
SIp
SIb
SI
OLD S2
S2
OLD S3
S3
OLD S4
S4

FIG. 7

individual pulse timing which corresponds to individual pulses of the clock signals CL1 and CL3, respectively, but these pulses occur at a rate which is a sub-multiple of the high frequency clock rate.

As is described in greater detail hereinafter, the operation of the control circuitry described herein determines whether a data transition occurs in the interval between the delays provided by an adjacent pair of the successive delay lines, there being four such intervals. There are correspondingly four possible choices of delays. The longest delay is, in essence, used only to provide an endpoint for the defined interval which corresponds to the longest of the delay lines which will be considered for possible selection.

At successive points in time determined by the period of the clock signals CL5 and CL6, the state of the output signal from each of the delay lines **21–25** is captured or sampled by a respective latch **31–35**. For each adjacent pair of successive delay lines, an EXCLUSIVE OR (XOR) gate is provided for combining the signals held in the respective latches, the gate output signals being designated ST1b–ST4b. As will be understood by those skilled in the art, a respective one of these gate output signals will be asserted if a data transition occurred in the interval between the successive delays provided by the two delay lines which feed that particular gate, in other words a discrepancy in the latched outputs of the respective delay lines caused by the occurence of a data signal transition in the interval defined by the two different delay values. Further, assuming that the clock rate for the data signal corresponds to the clock rate for the clock signals CL1–CL4, no more than one of the gate output signals will be asserted during each cycle of operation.

As will be understood by those versed in the art, the "asserted" state of a digital signal may be either the zero (low) or the one (high) state depending upon the logic scheme employed. In other words, the term "asserted" basically means that the necessary condition has been met. In the signal naming convention employed in FIGS. **1–5**, signals whose designations end with a "b" are low when asserted and the others are high when asserted.

While transitions in the incoming data signal and the clocking of the delay lines occurs at a very fast rate, the sampling accomplished by the latches and the operation of the rest of the control circuitry is driven at a slower clock rate to assure that the various sampling latches will reach stable states before decisions are made. As will also be understood by those skilled in the art, the fact that the delay lines provide progressive delays means a very increased likelihood that one of the phase shifted data signals will arrive at one of the latches just at the instant at which it is being clocked. Accordingly, it will also be understood that there exists a chance that the latch may be thrown into a metastable state from which a substantially increased time is required to settle.

The output signals from the XOR gates **36–39** are provided to a component sub-system conveniently designated as a FOUR-FLOP. This circuit, designated generally by reference character **41**, comprises four NAND gates which are interconnected to generate four signals no more than one of which can be asserted at any given time. As indicated previously, only one of the output signals from the XOR gates **36–39** should be asserted at any one time under normal circumstances, but the FOUR-FLOP **41** assures that no more than one signal is asserted.

As is explained in greater detail hereinafter, the one asserted output signal from the four-flop circuit **41** represents a possible choice for selecting one of the delayed data signals. In order to provide an operation which is stable and which provides a good, long-term (in a relative sense) choice for a compensating delay, the apparatus of FIG. **1** provides circuitry, designated generally at reference character **43**, for comparing each new possible choice with a previous or "candidate" choice. The system further comprises counter circuitry, designated generally by reference character **45**, for controlling the loading of new candidate choices and for changing the actual selection only after consistent behavior makes such changes logical. This latter process can be considered as one of integration or averaging.

Referring now to FIG. **5** which illustrates the comparison circuitry in greater detail, it may be seen that this subsystem comprises, along the left side of the drawing, four similar gate arrays, each of which comprises, at its lower portion, a ring memory or latch which is capable of holding a value applied to the respective input lead during successive operating cycles and, in the upper series of gates, means for applying new values to the memory element. Transfer or loading of a new possible choice originating in the FOUR-FLOP circuitry to the latches in the comparison circuitry is controlled by a signal designated LD (LOAD) and its complement LDb which are generated by the counter circuitry **45** as described hereinafter. For each of these four input and latch components there is also a corresponding XOR gate system which compares the new value with the old value. The respective XOR gates are designated by reference characters **51–54**. In one sense, the output signals from the XOR gates **51–54** may collectively be considered as a servo loop error signal which is used in automatically adjusting the selected value of delay as described hereinafter.

The signals generated in these first two sections of the comparison circuitry are logically combined in an array of gates designated generally by reference character **55** to generate signals, designated UP, DOWN and HOLD, which are provided to the counter circuitry **45** which provides averaging or integration as described previously. In general, it may be noted that the UP signal is generated when the new possible choice agrees with the held value; the DOWN signal is generated when the new possible choice disagrees with the held value; and the HOLD signal is generated if, within the current cycle of operation, no data transition has been detected.

The counter or integration circuitry **45** is implemented in the form of a shift register shown in greater detail in FIG. **6**. This circuitry is arranged so that, in effect, a single bit is shifted up and down a linear array of four similar stages. In general, the asserted bit is shifted upwards, i.e. to the right, when the UP signal is asserted and is shifted to the left, i.e. down, when the DOWN signal is asserted. It should be noted, however, that the gates generating the UP and DOWN signals (FIG. **6**) take into consideration the signal designated HOLD so that a bit is shifted neither up nor down during any cycle when the HOLD signal is asserted. As may be seen from FIG. **6**, the HOLD signal is generated as a NOR function of the four signals originating in the four-flop circuitry and representing the new possible choice. However, as is understood by those skilled in the art, a data stream comprising a succession of zeros or a succession of ones will not provide transitions

from the data utilization circuitry, said apparatus comprising:

a succession of delay lines providing progressively greater delays;

means for providing the arriving data signal to each of said delay lines thereby to obtain respective delayed data signals;

selector means for providing, to said utilization circuitry, a selected one of the delayed data signals;

means for comparing the delayed signals over a period of time and for setting said selector to a delayed data signal which is distant from the delayed data signals which bracket the most disparities.

6. Apparatus for adjusting the phase of data signals arriving at data utilization circuitry to adjust for uncontrollable phase shifts in the data signal originating apart from the data utilization circuitry, said apparatus comprising:

a plurality of delay lines providing progressively greater delays;

means for providing the arriving data signal to each of said lines thereby to obtain respective delayed data signals;

selector means, responsive to a selection value signal, for providing to said utilization circuitry one of said delayed data signals selected in accordance with said selection value;

respective latch means for acquiring and holding the instantaneous value of each said delayed data signal in response to a local clock signal;

respective gate means responsive to the latched values for generating a signal indicating whether a transition occurred between the respective delays provided by successively adjacent delay lines, the outputs of said gate means collectively representing a possible choice of delays;

means for comparing the gate generated signals over a period of time and for setting said selector to a delayed data signal which is distant from the delayed data signals which bracket the most transitions.

7. Apparatus for adjusting the phase of data signals arriving at data utilization circuitry to adjust for uncontrollable phase shifts in the data signal originating apart from the data utilization circuitry, said apparatus comprising:

a plurality of delay lines providing progressively greater delays;

means for providing the arriving data signal to each of said lines thereby to obtain respective delayed data signals;

selector means, responsive to a selection value signal, for providing to said utilization circuitry one of said delayed data signals selected in accordance with said selection value signal;

respective latch means for acquiring and holding the instantaneous value of each said delayed data signal in response to a local clock signal;

combinatorial logic means for combining the held data signals values to obtain signal representing degree of match;

state machine logic for generating and varying said selection signals as a function of said degree of match signal in a sense tending to select the delayed data signal furthest from disparities in adjacent data signals.

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